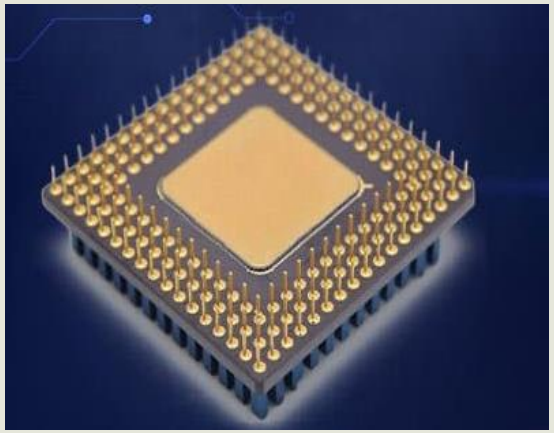


Microprocessor Architecture

Unit 1 Syllabus

Microprocessor Architecture and Memory Interface: Introduction, 8085 Microprocessor unit, 8085-Based Microcomputer, 8085 Machine Cycles & Bus Timings, Memory Interfacing, Interfacing the 8155 Memory Segment

Illustrative Example: Designing Memory for the MCTS Project, Testing and Troubleshooting Memory Interfacing Circuit, 8085- Based Single-Board microcomputer.

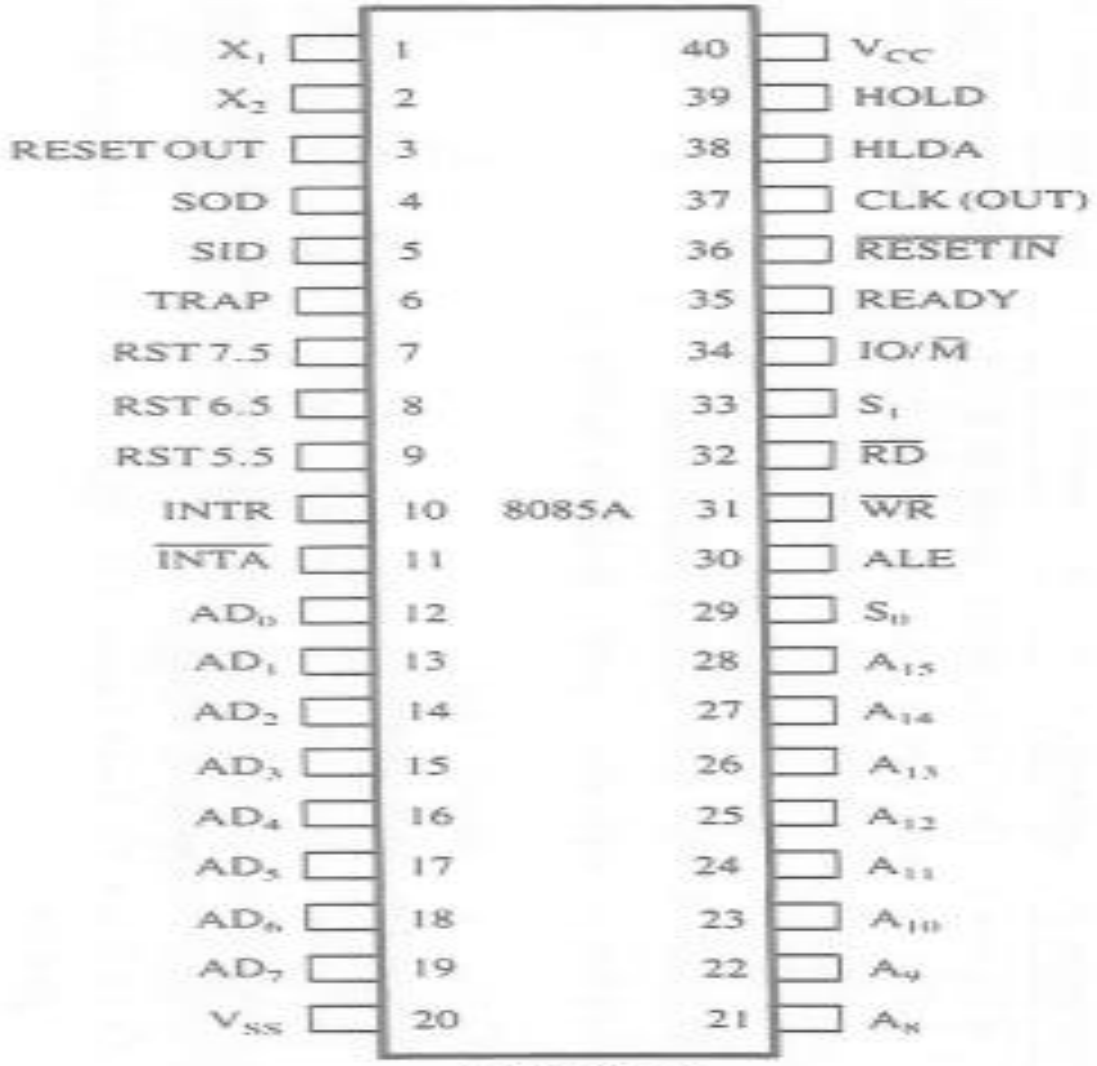
Microprocessor Architecture and Memory Interface

8085 Microprocessor

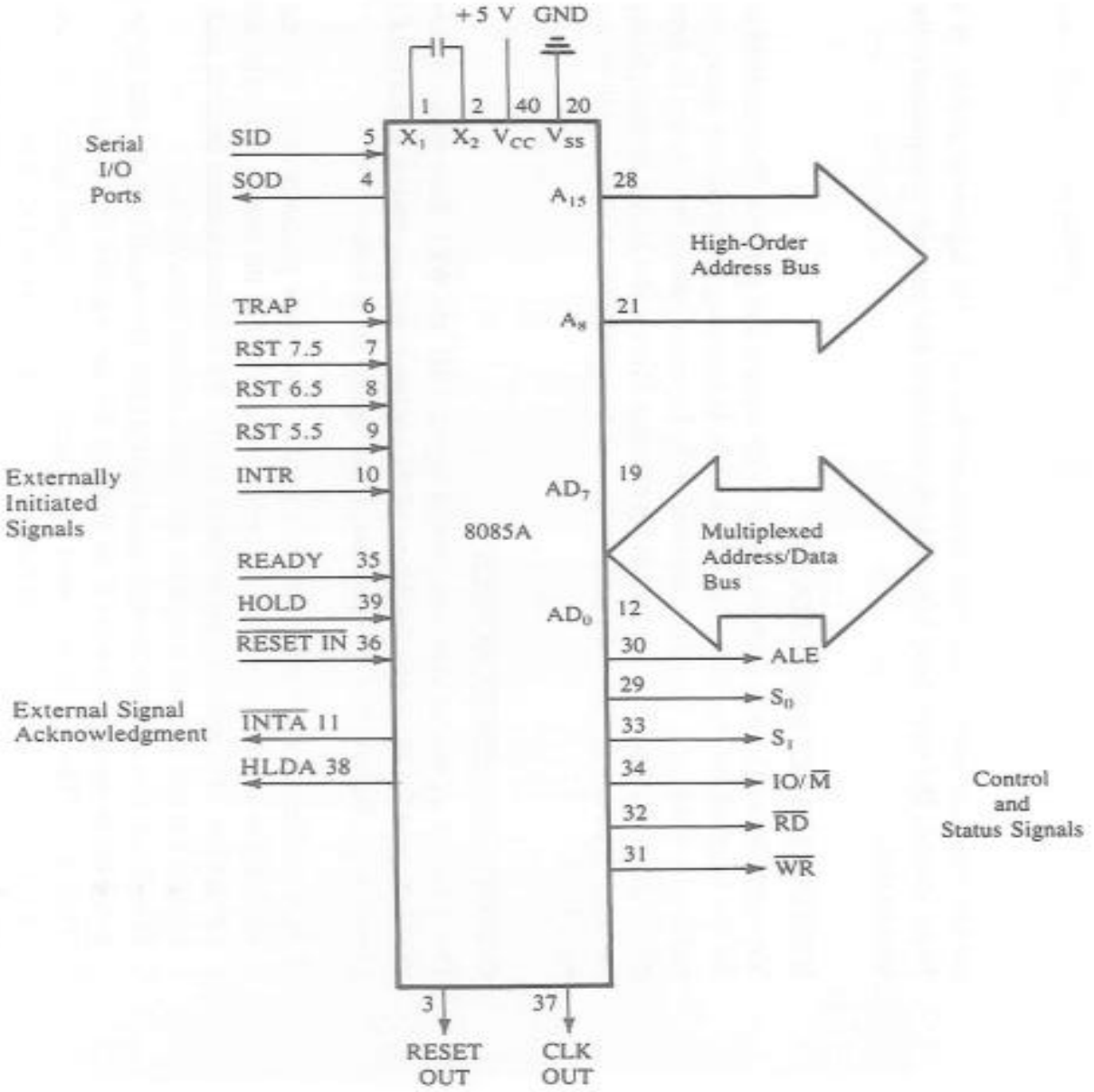
The 8085A (commonly known as the 8085) is an 8-bit general-purpose microprocessor capable of addressing 64K of memory. The device has forty pins, requires a +5 V single power supply, and can operate with a 3-MHz single-phase clock.

The 8085A-2 version can operate at the maximum frequency of 5 MHz.

All the signals can be classified into six groups: (1) address bus, (2) data bus, (3) control and status signals, (4) power supply and frequency signals, (5) externally initiated signals, and (6) serial I/O ports.


X1 1
X2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
VSS 20
8085A
40 VCC
39 HOLD
38 HLDA
37 CLK (OUT)
36 RESET IN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

8085 Pinout


+5 V
GND
1
2
40
20
X1
X2
VCC
VSS
Serial I/O Ports
SID 5
SOD 4
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
Externally Initiated Signals
INTR 10
READY 35
HOLD 39
RESET IN 36
External Signal Acknowledgment
INTA 11
HLDA 38
8085A
A15 28
A8 21
High-Order Address Bus
AD7 19
AD0 12
Multiplexed Address/Data Bus
30 ALE
29 S0
33 S1
34 IO/M
32 RD
31 WR
Control and Status Signals
3
37
RESET OUT
CLK OUT

ADDRESS BUS

The 8085 has 16 signal lines (pins) that are used as the address bus; however, these lines are split into two segments: A_{15}- A_8 and AD_7- AD_0 . The eight signal lines, A_{15}- A_8 are unidirectional and used for the most significant bits, called the high-order address, of a 16-bit address.

MULTIPLEXED ADDRESS/DATA BUS

The signal lines AD_7- AD_0, are bidirectional: they serve a dual purpose. They are used as the low-order address bus as well as the data bus. In executing an instruction, during the earlier part of the cycle, these lines are used as the low-order address bus. During the later part of the cycle, these lines are used as the data bus. (This is also known as multiplexing the bus.) However, the low-order address bus can be separated from these signals by using a latch.

- **CONTROL AND STATUS SIGNALS**
- This group of signals includes two control signals (RD and WR), three status signals (IO/M, S_1 and S_0) to identify the nature of the operation, and one special signal (ALE) to indicate the beginning of the operation. These signals are as follows:
- ALE-Address Latch Enable: This is a positive going pulse generated every time the 8085 begins an operation (machine cycle); it indicates that the bits on AD_7- AD_0 are address bits. This signal is used primarily to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines, A_7- A_0

RD-Read: This is a Read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

WR-Write: This is a Write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

IO/M: This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation; when it is low, it indicates a memory operation. This signal is combined with RD (Read) and WR (Write) to generate I/O and memory control signals.

- S_1 and S_0 : These status signals, similar to IO/M, can identify various operations, but they are rarely used in small systems.

POWER SUPPLY AND CLOCK FREQUENCY

- The power supply and frequency signals are as follows:
- V_{cc} : +5V power supply.
- V_{ss} : Ground Reference.
- X_1, X_2 : A crystal (or RC, LC network) is connected at these two pins. The frequency is internally divided by two; therefore, to operate a system at 3 MHz, the crystal should have a frequency of 6 MHz.
- CLK (OUT)-Clock Output: This signal can be used as the system clock for other devices.

- **EXTERNALLY INITIATED SIGNALS, INCLUDING INTERRUPTS**
- The 8085 has five interrupt signals that can be used to interrupt a program execution. One of the signals, INTR (Interrupt Request), is identical to the 8080A micro- processor interrupt signal (INT); the others are enhancements to the 8080A. The micro- processor acknowledges an interrupt request by the INTA (Interrupt Acknowledge) signal.
- In addition to the interrupts, three pins-RESET, HOLD, and READY-accept the externally initiated signals as inputs. To respond to the HOLD request, the 8085 has one signal called HLDA (Hold Acknowledge).

- RESET IN: When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated, and the MPU is reset.
- RESET OUT: This signal indicates that the MPU is being reset. The signal can be used to reset other devices.
- **SERIAL I/O PORTS**
- The 8085 has two signals to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data). In serial transmission, data bits are sent over a single line, one bit at a time, such as the transmission over telephone lines.

Microprocessor Communication and Bus Timing

To fetch the byte, the MPU per- forms the following steps:

- Step 1: The microprocessor places the 16-bit memory address from the program counter (PC) on the address bus (Figure 4.2).
- Figure 4.3 shows that at T_1, the high-order memory address 20H is placed on the ad- dress lines A_{15}-A_8, the low-order memory address 05H is placed on the bus AD_7-AD_0 and the ALE signal goes high. Similarly, the status signal IO/M goes low, indicating that this is a memory-related operation
- Step 2: The control unit sends the control signal RD to enable the memory chip (Figure 4.2). The control signal RD is sent out during the clock period T_2, thus enabling the memory chip (Figure 4.3). The RD signal is active during two clock periods.

- Step 3: The byte from the memory location is placed on the data bus.
- When the memory is enabled, the instruction byte (4FH) is placed on the bus AD_7-AD_0 and transferred to the microprocessor. The RD signal causes 4FH to be placed on bus AD_7-AD_0 (shown by the arrow), and when RD goes high, it causes the bus to go into high impedance.
- Step 4: The byte is placed in the instruction decoder of the microprocessor, and the task is carried out according to the instruction.
- The machine code or the byte (4FH) is decoded by the instruction decoder, and the contents of the accumulator are copied into register C. This task is performed during the period T_4 in Figure 4.3.

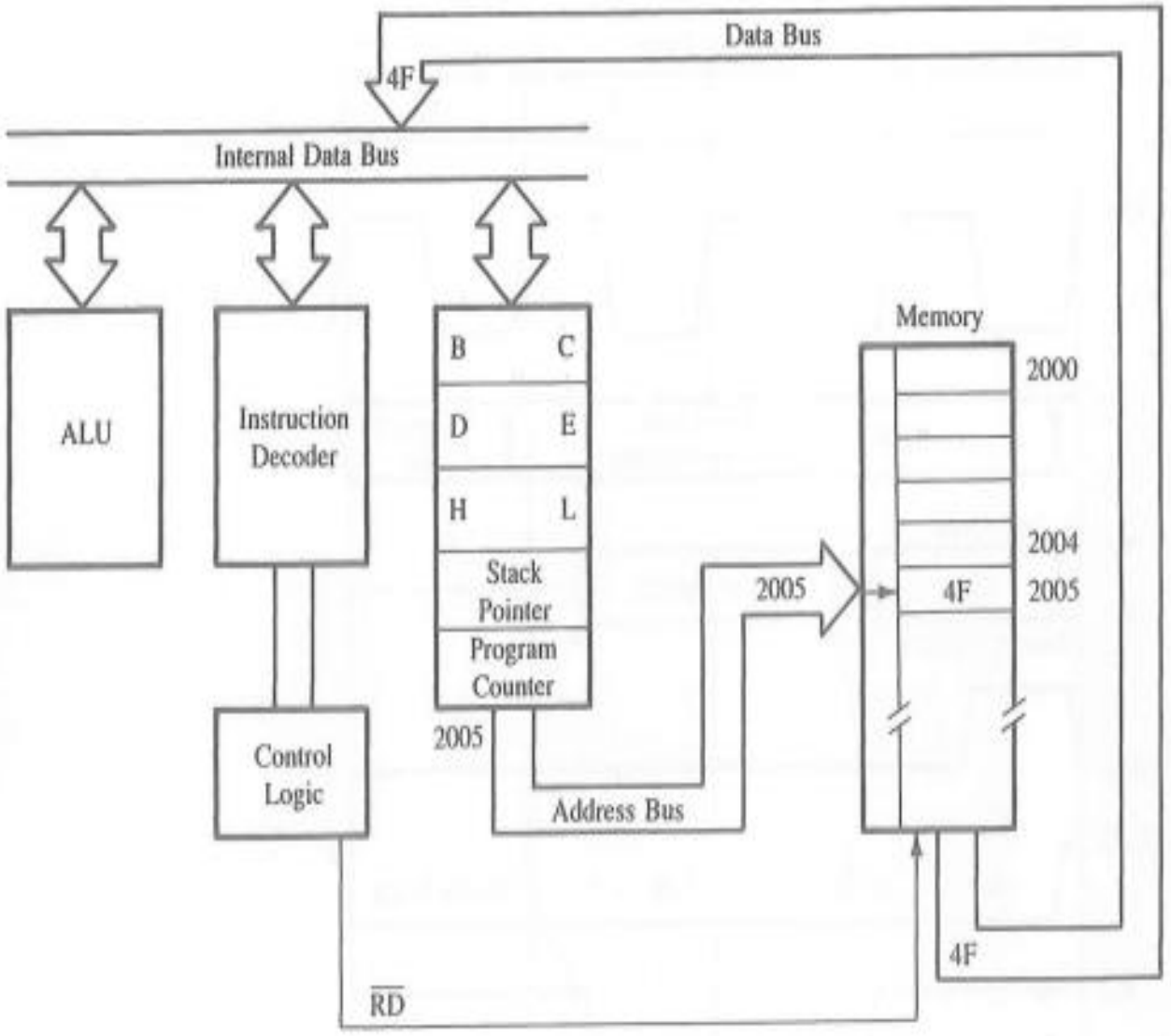


FIGURE 4.2
Data Flow from Memory to the MPU

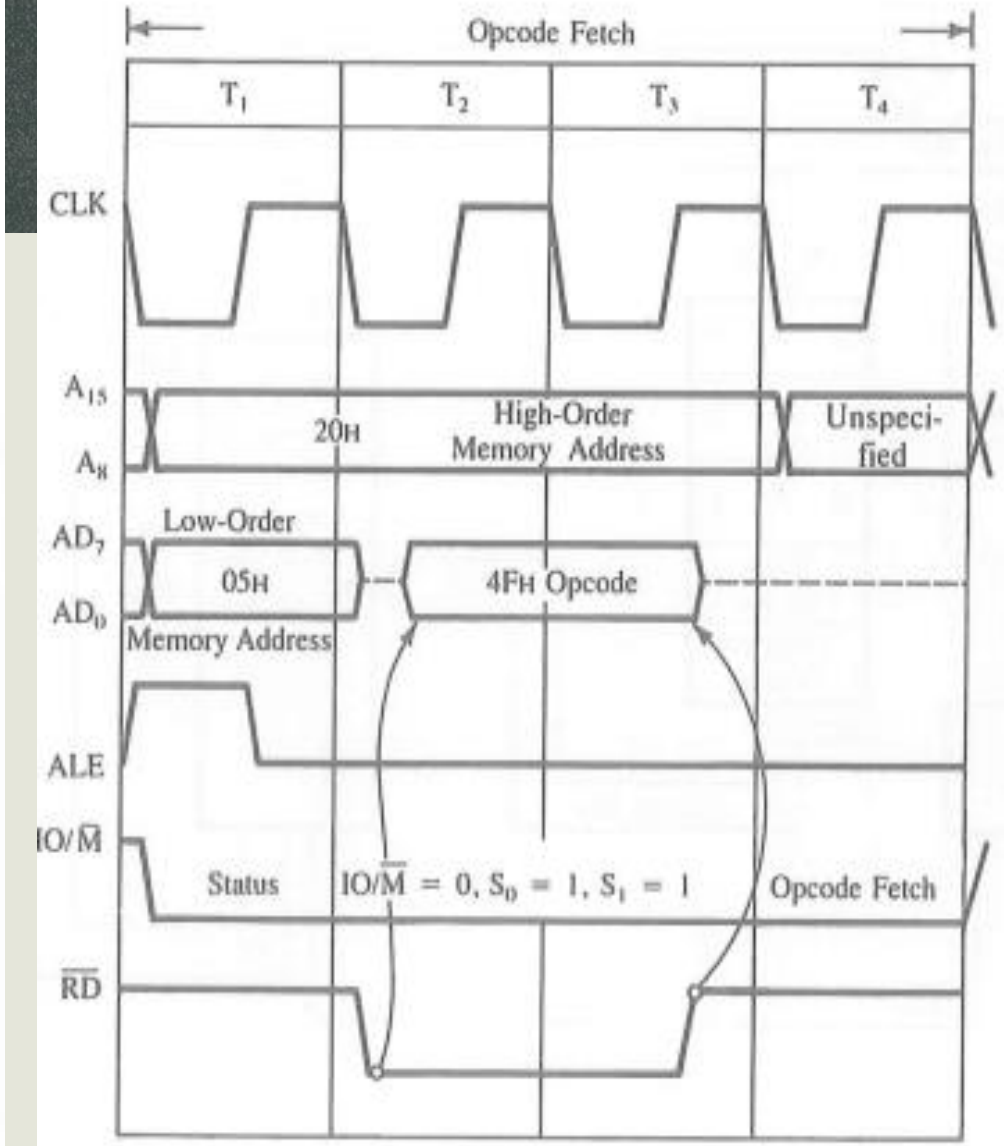


FIGURE 4.3
Timing: Transfer of Byte from Memory to MPU

Demultiplexing the bus AD_7- AD_0

- The address on the high-order bus (20H) remains on the bus for three clock periods. However, the low-order address (05H) is lost after the first clock period. This address needs to be latched and used for identifying the memory address. If the bus AD_7- AD_0, is used to identify the memory location (2005H), the ad- dress will change to 204FH after the first clock period.
- Figure 4.4 shows a schematic that uses a latch and the ALE signal to demultiplex the bus. The bus AD_7- AD_0, is connected as the input to the latch 74LS373. The ALE signal is connected to the Enable (G) pin of the latch, and the Output control (OC) signal of the latch is grounded.
- Figure 4.3 shows that the ALE goes high during T_1. When the ALE is high, the latch is transparent; this means that the output changes according to input data. During T1, the output of the latch is 05H. When the ALE goes low, the data byte 05H is latched until the next ALE, and the output of the latch represents the low-order address bus A_7- A_0 after the latching operation.

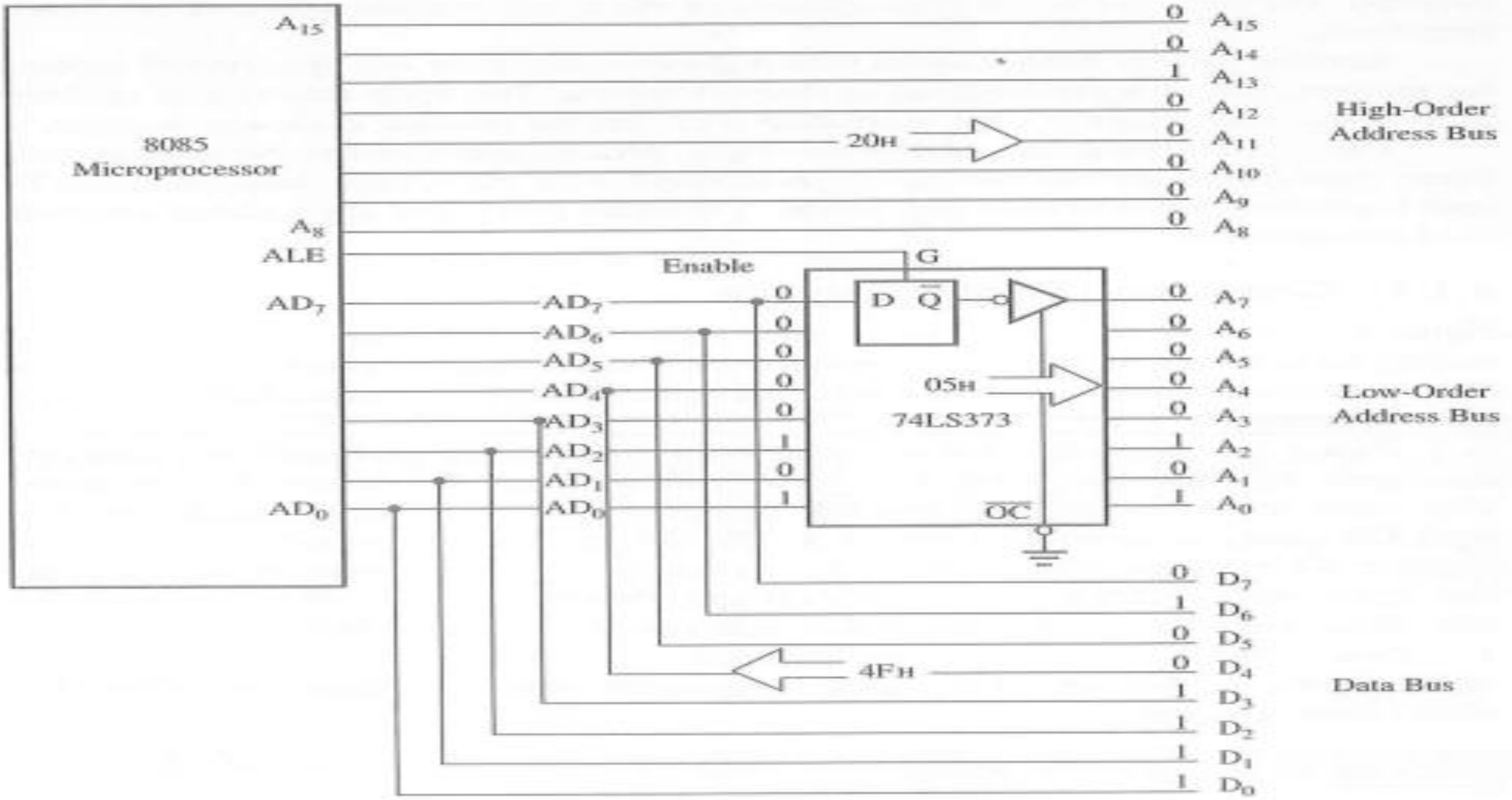


FIGURE 4.4
Schematic of Latching Low-Order Address Bus

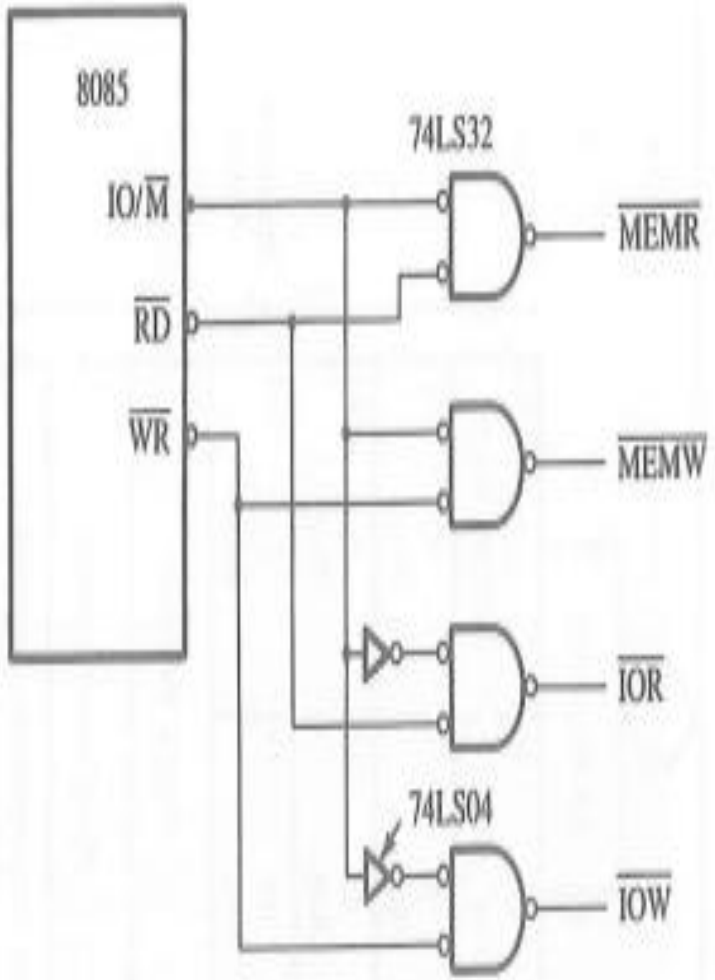
After carefully examining Figure 4.3, we can make the following observations:

- 1. The machine code 4FH (0100 1000) is a one-byte instruction that copies the contents of the accumulator into register C.
- 2. The 8085 microprocessor requires one external operation-fetching a machine code* from memory location 2005H.
- 3. The entire operation-fetching, decoding, and executing requires four clock periods.
- Now we can define three terms-instruction cycle, machine cycle, and T-state-and use these terms later for examining timings of various 8085 operations
- Instruction cycle is defined as the time required to complete the execution of an instruction. The 8085 instruction cycle consists of one to six machine cycles or one to six operations.
- Machine cycle is defined as the time required to complete one operation of accessing memory, I/O, or acknowledging an external request. This cycle may consist of three to six T-states. In Figure 4.3, the instruction cycle and the machine cycle are the same.
- T-state is defined as one subdivision of the operation performed in one clock period. These subdivisions are internal states synchronized with the system clock, and each T- state is precisely equal to one clock period. The terms T-state and clock period are often used synonymously.

Generating Control Signals

- Figure 4.3 shows the RD (Read) as a control signal. Because this signal is used both for reading memory and for reading an input device, it is necessary to generate two different Read signals: one for memory and another for input. Similarly, two separate Write signals must be generated.
- Figure 4.5 shows that four different control signals are generated by combining the signals RD, WR, and IO/M. The signal IO/M goes low for the memory operation. This signal is ANDed with RD and WR signals by using the 74LS32 quadruple two- input OR gates, as shown in Figure 4.5. The OR gates are functionally connected as negative NAND gates. When both input signals go low, the outputs of the gates go low and generate MEMR (Memory Read) and MEMW (Memory Write) control signals. When the IO/M signal goes high, it indicates the peripheral I/O operation. Figure 4.5 shows that this signal is complemented using the Hex inverter 74LS04 and ANDed with the RD and WR signals to generate IOR (I/O Read) and IOW (I/O Write) control signals.
- To demultiplex the bus and to generate the necessary control signals, the 8085 microprocessor requires a latch and logic gates to build the MPU, as shown in Figure 4.6. This MPU can be interfaced with any memory or I/O.

FIGURE 4.5
Schematic to Generate Read/Write Control Signals for Memory and I/O



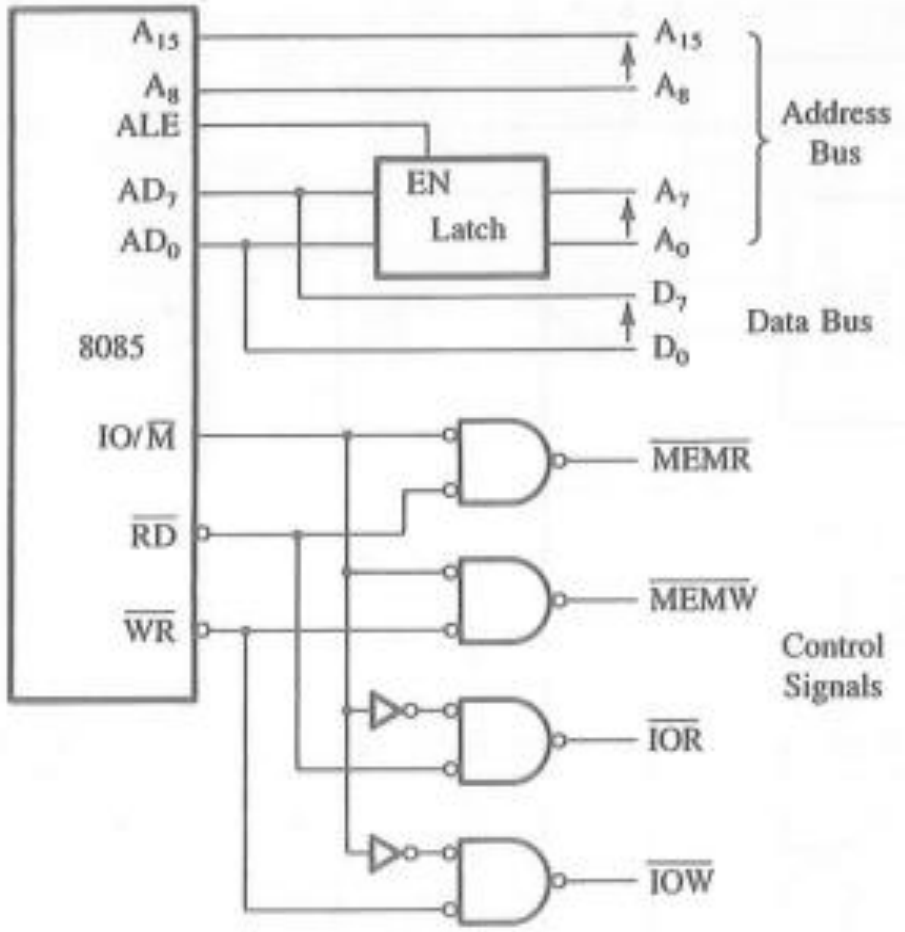


FIGURE 4.6
8085 Demultiplexed Address and Data Bus with Control Signals

THE ALU

- The arithmetic/logic unit performs the computing functions; it includes the accumulator, the temporary register, the arithmetic and logic circuits, and five flags. The temporary register is used to hold data during an arithmetic/logic operation. The result is stored in the accumulator, and the flags (flip-flops) are set or reset according to the result of the operation.

- The flags are affected by the arithmetic and logic operations in the ALU. In most of these operations, the result is stored in the accumulator. Therefore, the flags generally reflect data conditions in the accumulator with some exceptions. The descriptions and conditions of the flags are as follows:

- S-Sign flag: After the execution of an arithmetic or logic operation, if bit D_7, of the result (usually in the accumulator) is 1, the Sign flag is set. This flag is used with signed numbers. In a given byte, if D_7 is 1, the number will be viewed as a negative number; if it is 0, the number will be considered positive. In arithmetic operations with signed numbers, bit D_7, is reserved for indicating the sign, and the remaining seven bits are used to represent the magnitude of a number. However, this flag is irrelevant for the operations of unsigned numbers. Therefore, for unsigned numbers, even if bit D_7, of a result is I and the flag is set, it does not mean the result is negative. (See Appendix A2 for a discussion of signed numbers.)

- Z-Zero flag: The Zero flag is set if the ALU operation results in 0, and the flag is re- set if the result is not 0. This flag is modified by the results in the accumulator as well as in the other registers.

- AC-Auxiliary Carry flag: In an arithmetic operation, when a carry is generated by digit D_3, and passed on to digit D_4, the AC flag is set. The flag is used only internally for BCD (binary-coded decimal) operations and is not available for the programmer to change the sequence of a program with a jump instruction.
- P-Parity flag: After an arithmetic or logical operation, if the result has an even number of Is, the flag is set. If it has an odd number of 1s, the flag is reset. (For example, the data byte 0000 0011 has even parity even if the magnitude of the number is odd.)
- CY-Carry flag: If an arithmetic operation results in a carry, the Carry flag is set; otherwise it is reset. The Carry flag also serves as a borrow flag for subtraction.

The bit positions reserved for these flags in the flag register are as follows:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

Among the five flags, the AC flag is used internally for BCD arithmetic; the instruction set does not include any conditional jump instructions based on the AC flag. Of the remaining four flags, the Z and CY flags are those most commonly used.

TIMING AND CONTROL UNIT

This unit synchronizes all the microprocessor operations with the clock and generates the control signals necessary for communication between the microprocessor and peripherals. The control signals are similar to a sync pulse in an oscilloscope. The RD and WR signals are sync pulses indicating the availability of data on the data bus.

INSTRUCTION REGISTER AND DECODER

The instruction register and the decoder are part of the ALU. When an instruction is fetched from memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events to follow. The instruction register is not programmable and cannot be accessed through any instruction.

REGISTER ARRAY

The programmable registers were discussed in the last chapter. Two additional registers, called temporary registers W and Z, are included in the register array. These registers are used to hold 8-bit data during the execution of some instructions. However, because they are used internally, they are not available to the programmer.

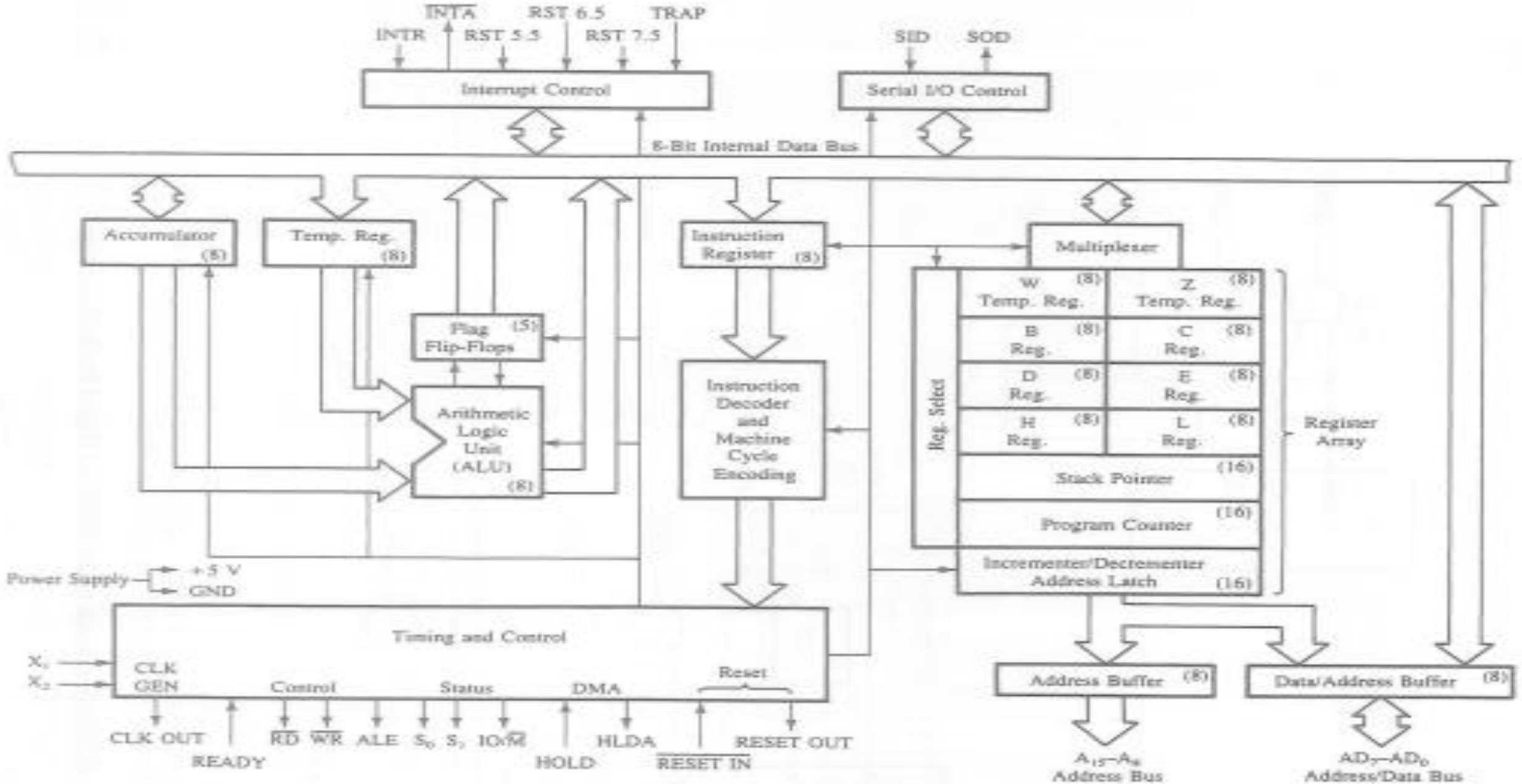


FIGURE 4.2
The 8085A Microprocessor: Functional Block Diagram

Decoding and executing an instruction

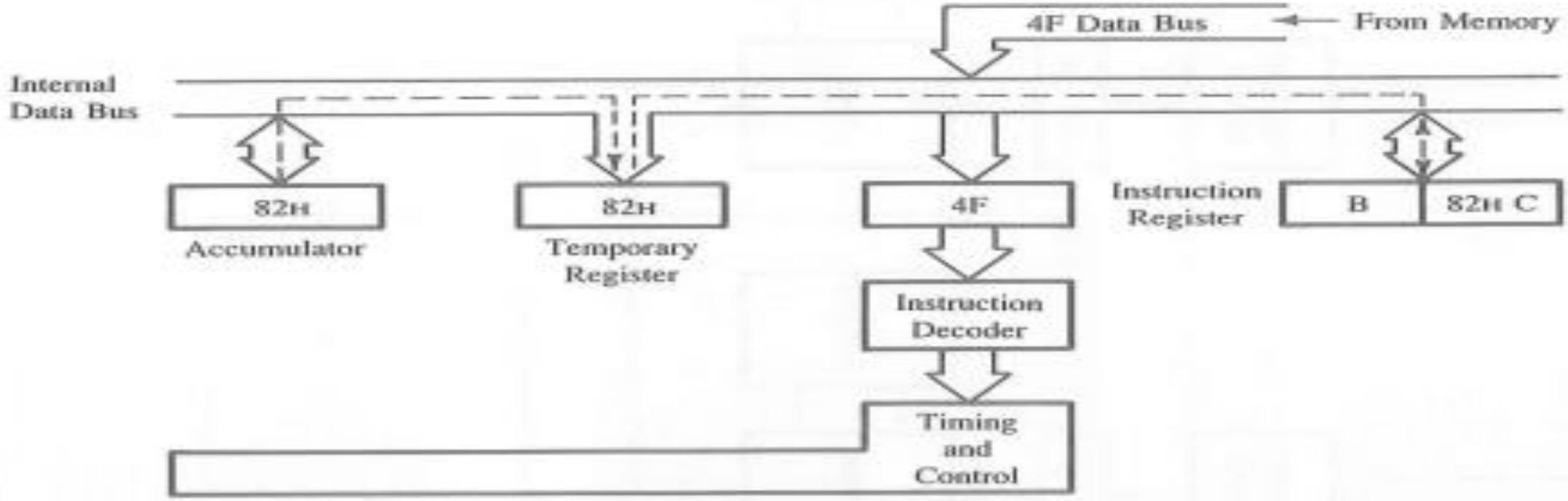


FIGURE 4.8
Instruction Decoding and Execution

8085 Machine Cycle and Bus Timing

- The 8085 microprocessor is designed to execute 74 different instruction types.
- Each instruction has two parts: operation code, known as opcode, and operand. The opcode is a command such as Add, and the operand is an object to be operated on, such as a byte or the contents of a register. Some instructions are 1-byte instructions and some are multi- byte instructions. To execute an instruction, the 8085 needs to perform various operations such as Memory Read/Write and I/O Read/Write.
- Basically, the microprocessor external communication functions can be divided into three categories:
- 1. Memory Read and Write
- 2. I/O Read and Write
- 3. Request Acknowledge
- These functions are further divided into various operations (machine cycles), as shown in Table 4.1. Each instruction consists of one or more of these machine cycles, and each machine cycle is divided into T-states.

Opcode Fetch Machine Cycle

- The first operation in any instruction is Opcode Fetch. The microprocessor needs to get (fetch) this machine code from the memory register where it is stored before the microprocessor can begin to execute the instruction.
- However, to differentiate an opcode from a data byte or an address, this machine cycle is identified as the Opcode Fetch cycle by the status signals (IO/M = 0, S_1= 1, S_0 = 1); the active low IO/M signal indicates that it is a memory operation, and S, and S, being high indicate that it is an Opcode Fetch cycle.
- This Opcode Fetch cycle is called the M_1, cycle and has four T-states. The 8085 uses the first three states T_1-T_3, to fetch the code and T_4 to decode and execute the opcode. In the 8085 instruction set, some instructions have opcodes with six T-states.